

MODE ENTRY CIRCUIT AND METHOD

TECHNICAL FIELD

The present invention is related generally to the field of semiconductor memory devices, and more particularly, to circuitry included therein for generating test mode enable signals.

BACKGROUND OF THE INVENTION

In many memory devices, flexibility is added through the use different modes of operation in which the memory device can operate. Through the use of different operating modes, the memory device can perform operations or functions not typically desired by a user, but provide additional capabilities that may found desirable by memory device designers and manufacturers. For example, one popular mode of operation is the non-user test mode which provides additional test functionality that facilitates the testing of the memory devices.

There are many well known approaches to invoking the different modes of operation of a memory device. For example, entry into the test modes is often made by way of applying a relatively high-voltage signal to an input pin or pins of the memory device. The point at which the test mode is invoked, that is, the trigger voltage, is typically measured relative to a voltage source, such as the device supply voltage VCC or the input/output supply voltage VCCQ. Shown in Figure 1 is a typical arrangement of circuitry 100 that is used to determine if a test mode has been invoked through the application of a relatively high-voltage to a device input pad, and in response, generate an output signal having a voltage level indicative of whether the test mode should be entered. The circuitry 100 includes a high-voltage detector 110 to which a reference voltage 112 and an input signal 114 are applied. As illustrated in Figure 1, the reference voltage 112 is the device supply voltage VCC and the input signal 114 is an input signal PAD from a device input pad. The HV detector 110 compares the voltage of the PAD signal to VCC or a voltage

level related to VCC, and in response, produces a test enable signal TEST_EN having a voltage indicating whether the test mode should be entered. The TEST_EN signal can then be used to place the device into a test mode. The design and implementation of HV detectors, such as the HV detector 110, are known in the art.

5 A problem with previously discussed approach of test mode entry, however, is that noisy signals or dramatic voltage variations in the signals applied to input pads of a memory device may inadvertently trigger entry into a test mode. Operation of the memory device after accidentally entering into such a mode by a user could irreparably damage the part. Consequently, the test mode entry voltage should be set high enough to avoid
10 inadvertent test mode entry.

Further complicating the issue, however, is the fact that it may be desirable for the test mode entry voltage to be lower than that which will ensure a test mode is not inadvertently entered, such as in the following case. In order to increase test throughput, memory devices, test programs, and test equipment have been designed to perform device
15 testing more efficiently. For example, memory devices have been designed to test multiple blocks of memory in parallel, thus avoiding the testing of memory cells one at a time. Additionally, test programs have been written to take advantage of the parallel testing capabilities provided by the memory devices, and test equipment have been modified to increase the number of devices that can be tested concurrently by the test equipment.
20 However, the number of devices that can be tested concurrently may be limited by test equipment limitations. For example, memory testers typically have limited high-voltage drive capabilities. Thus, where high-voltage signals are applied during testing, the number of devices that can be tested concurrently will be limited. In the particular case where the high-voltage drive capabilities of the test equipment is limited, the test entry voltage should
25 be reduced to accommodate this limitation. However, with the conventional high-voltage detection circuitry previously discussed with respect to Figure 1, where the test mode entry voltage is based on one voltage, such as VCC, lowering the mode trigger voltage increases the likelihood that test mode will be entered inadvertently.

Additionally, many memory devices are designed to operate over a range of power supply voltages. In some cases, the device supply voltage and the input/output supply voltage can be at different voltage levels. Where this is the case, having the test mode entry voltage level based on one voltage, such as the device supply voltage, may 5 significantly reduce the margin between the acceptable voltage levels of input signals and the test mode trigger voltage.

An approach to decreasing the likelihood of inadvertently entering a test mode, where entry is made through the application of high-voltage signals, is provided in U.S. Patent No. 5,526,364 to Roohparvar. As described therein, high-voltage signals are 10 applied to two or more input pins of the memory device to enter into a test mode. However, as previously discussed, where the test equipment has limited high-voltage drive capability, driving multiple pins to sufficient voltage levels to enter into the test modes will reduce the number of devices that can be tested concurrently. Thus, the approach described in the aforementioned patent may not provide an acceptable alternative.

15 Therefore, there is a need for an alternative apparatus and method that can be used to generate test mode entry signals in response to an input signal.

SUMMARY OF THE INVENTION

The present invention is directed to an apparatus and method for generating a mode activation signal in response to an input signal having a voltage exceeding the 20 greater of two reference voltages by a voltage margin. The apparatus includes a voltage detector having an input for receiving the input signal, and first and second reference inputs for receiving first and second reference voltages, respectively. The voltage detector further includes an output at which an active mode activation signal is provided in response to the voltage of the input signal exceeding the greater of the voltages of the first and second 25 reference voltages power supplies by a voltage margin.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a conventional test mode entry circuit.

Figure 2 is a block diagram of a mode entry circuit according to an embodiment of the present invention.

5 Figure 3 is a schematic drawing of a high-voltage detector according to an embodiment of the present invention that may be used in the mode entry circuit of Figure 2.

Figure 4 is a block diagram of a memory device including the mode entry circuit of Figure 2.

Figure 5 is a block diagram of a computer system including the memory
10 device of Figure 4.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention are directed to a mode entry circuit that generates an enable signal in response to the voltage of an input signal exceeding the greater of at least two references voltages. Certain details are set forth below to provide a
15 sufficient understanding of the invention. However, it will be clear to one skilled in the art that the invention may be practiced without these particular details. In other instances, well-known circuits, control signals, and timing protocols have not been shown in detail in order to avoid unnecessarily obscuring the invention.

Figure 2 illustrates a mode entry circuit 200 according to an embodiment of
20 the present invention. The test mode entry circuit 200 includes a first high-voltage (HV) detector 204 having a reference voltage input 206 coupled to a device power supply VCC, and further includes a second HV detector 208 having a reference voltage input 210 coupled to an input/output power supply VCCQ. Both the HV detectors 204, 208 have an input 212 coupled to receive a signal PAD applied to an external device pad 214. The
25 output of the HV detectors 204, 208 are provided to an AND gate 220 having an output at which a mode enable signal MODE_EN is provided.

In operation, each of the HV detectors 204, 208 provides a HIGH output signal in response to the voltage of the PAD signal exceeding the voltage of the respective reference voltages by a voltage margin. Consequently, an active MODE_EN signal is output by the AND gate 220 when the voltage of the PAD signal exceeds both the voltage of VCC and VCCQ by the voltage margin. From an alternative perspective, an active MODE_EN signal is provided when the voltage of the PAD signal exceeds the greater of VCC or VCCQ by the voltage margin. It will be appreciated that the voltage margin can be adjusted accordingly. In some instances, if desired, the voltage margin can be reduced to zero, thus mode entry will be made when the voltage of the PAD signal exceeds the greater of VCC or VCCQ. Additionally, it is not necessary for the voltage margins of the HV detectors 204, 208 to be the same.

By having the generation of an active MODE_EN signal based on the greater of two voltages, the likelihood of inadvertent entry into a mode of operation in a device designed to operate at various power supply voltages can be reduced when compared to the conventional test mode circuit illustrated in Figure 1. At the same time, the mode entry circuit 200 allows for lower VCC and VCCQ supply voltages can be used during testing of the devices to accommodate test equipment limitations.

For example, as previously mentioned, it is generally desirable during the testing of a device to set the voltage of both VCC and VCCQ to a lower operating voltage to account for test equipment limitations, such as limited high-voltage drive capabilities. Entry into a mode of operation is then made through the application of a PAD signal having a relatively high voltage with respect to the lower operating voltages of VCC and VCCQ. However, where the device will then be used in an environment that requires two different power supply voltages, such as when the voltage of VCCQ is greater than VCC, the likelihood of inadvertent entry into a mode of operation increases in the conventional case because mode entry based on the voltage of a PAD signal is with respect to only VCC or only VCCQ. That is, in the case where the mode trigger voltage is based on only VCC, and VCCQ is greater than VCC, variations in the voltage of a PAD signal, which has a voltage

level based on VCCQ, may be large enough to exceed the trigger voltage, and a mode of operation will be inadvertently entered. However, simply raising the mode trigger voltage to prevent inadvertent entry into a mode of operation reintroduces the problems associated with limitations in test equipment.

5 In contrast, the mode entry circuit 200 avoids the aforementioned problem because generation of the MODE_EN signal is based on the greater of two voltages, such as VCC and VCCQ, and not one or the other. Thus, with a device including the mode entry circuit 200, testing of the device can be made with both VCC and VCCQ at the lower operating voltage, and when the device is required to operate at two different supply
10 voltages, the mode trigger voltage will be adjusted to accommodate the increased voltage of whichever power supply has the greater voltage. With the mode entry circuit 200, either the VCC or VCCQ power supply can have a higher voltage and the mode trigger voltage will change accordingly. For example, in the previous example, VCCQ was greater than VCC, and entry into a mode of operation was made by applying a PAD signal having a
15 voltage that exceeded VCCQ by a voltage margin. However, if the situation arises where it is desirable to have VCC greater than VCCQ, entry into a mode of operation will be made if the voltage of the PAD signal exceeds the voltage of VCC by a voltage margin.

Figure 3 illustrates a HV detector 300 that can be substituted for the HV detectors 204, 208 of Figure 2. As illustrated in Figure 3, the HV detector 300 includes
20 enable circuitry formed from an inverter 301 that receives a circuit enable signal EN_N, which as illustrated in Figure 3 is active when the signal is LOW. The enable circuitry also includes an NMOS transistor 303 and a PMOS transistor 305, which are both switched ON when the EN_N signal is LOW. The EN_N signal is provided by control circuitry (not shown) that generates the appropriate EN_N signal in response to external memory
25 commands. The generation of such an EN_N signal is well known in the art. It will be appreciated that the enable circuitry illustrated in Figure 3 can be modified, or even eliminated from the HV detector 300 without departing from the scope of the present invention.

The HV detector 300 further includes a voltage comparator stage 304. The voltage comparator stage includes both PMOS load elements 304 and NMOS load elements 306 to set the mode trigger voltage relative to the input reference voltage REFVC. It will be appreciated that adjusting the dimensions of the PMOS and NMOS load elements 304, 306 will change the mode trigger voltage. However, those of ordinary skill have sufficient understanding of the art to use alternative means to adjust the mode trigger voltage. An output signal HVDETECT is provided by the voltage comparator stage 304 at an output 310. In the case where PAD does not exceed REFVC by the voltage margin set by the PMOS and NMOS load elements 304, 306, the transistor 340 remains OFF and the output 10 310 is held LOW through NMOS transistors 312 and 303. However, if the voltage of REFVC exceeds the voltage of REFVC by the voltage margin, the transistor 340 is switched ON, and pulls the output 310 HIGH to provide an active HVDETECT signal. The HVDETECT signal is provided to the input of a Schmitt trigger 320. The hysteresis of the Schmitt trigger 320 prevents its output from switching from minor voltage variations in 15 the HVDETECT signal that may result from variations in either the PAD or REFVC signals.

A two-input NOR gate 330 is coupled to receive the output of the Schmitt trigger 330 and the EN_N signal. As mentioned previously, the EN_N signal is active when LOW. Consequently, when the EN_N signal is active, the logic state of the output 20 signal from the Schmitt trigger 330 is inverted by the NOR gate 330 to provide an output signal PADHV that is HIGH when the voltage of the PAD signal exceeds the voltage of the REFVC signal by at least the voltage margin established by the PMOS and NMOS load elements 304, 306. Otherwise, the PADHV signal is LOW. As illustrated in Figure 2, the PADHV signal is provided to AND gate 220, which in turn generates the MODE_EN 25 signal. Although Figure 3 illustrates a particular HV detector 300, it will be appreciated that alternative HV voltage detection circuitry can be used in the mode entry circuit 200 without departing from the scope of the present invention. Such alternative voltage detection circuitry are well known by those ordinarily skilled in the art.

Figure 4 illustrates a non-volatile memory device 400 including a mode entry circuit 414 according to an embodiment of the present invention incorporated therein. Commands are issued to a command state machine (CSM) 404 which acts as an interface between the an external processor (not shown) and an internal write state machine (WSM) 408. When a specific command is issued to the CSM 404, internal command signals are provided to the WSM 408, which in turn, executes the appropriate algorithm to generate the necessary timing signals to control the memory device 400 internally, and accomplish the requested operation. The CSM 404 also provides the internal command signals to an ID register 408 and a status register 410, which allows the progress of various operations to be monitored when interrogated by issuing to the CSM 404 the appropriate command.

Portions of the commands are also provided to input/output (I/O) logic 412 which, in response to a read or write command, enables the data input buffer 416 and the output buffer 418, respectively. The I/O logic 412 also provides signals to the address input buffer 422 in order for address signals to be latched by an address latch 424. The latched address signals are in turn provided by the address latch 424 to an address multiplexer 428 under the command of the WSM 406. The address multiplexer 428 selects between the address signals provided by the address latch 424 and those provided by an address counter 432. The address signals provided by the address multiplexer 428 are used by an address decoder 440 to access the memory cells of a memory bank 444 that correspond to the address signals. A gating/sensing circuit 448 is coupled to the memory bank 444 for the purpose of programming and erase operations, as well as for read operations.

During a read operation, data is sensed by the gating/sensing circuit 448 and amplified to sufficient voltage levels before being provided to an output multiplexer 450. The read operation is completed when the WSM 406 instructs the output buffer 418 to latch data provided from the output multiplexer 450 to be provided to the extern processor. The output multiplexer 450 can also select data from the ID and status registers 408, 410 to be provided to the output buffer 418 when instructed to do so by the WSM 406. During a

program or erase operation, the I/O logic 412 commands the data input buffer 416 to provide the data signals to a data register 460 to be latched. The WSM 406 also issues commands to program/erase circuitry 464 which uses the address decoder 440 to carry out the process of injecting or removing electrons from the memory cells of the memory bank 5 444 to store the data provided by the data register 460 to the gating sensing circuit 448. To ensure that sufficient programming or erasing has been performed, a data comparator 470 is instructed by the WSM 406 to compare the state of the programmed or erased memory cells to the data latched by the data register 460.

As illustrated in Figure 4, the address signals are also provided to the mode 10 entry circuit 414 to initiate a mode of operation through the application of a relatively high voltage signal. An active mode enable signal is generated by the mode entry circuit 414 in response to an address signal or signals having the sufficient voltage level, and is provided to the CSM 404 and the I/O logic 412 to indicate that a mode of operation has been triggered. The CSM 404 and the I/O logic 412 then generate the appropriate internal 15 command and timing signals to initiate the mode of operation.

It will be appreciated that the embodiment of the memory device 400 that is illustrated in Figure 4 has been provided by way of example and that the present invention is not limited thereto. Those of ordinary skill in the art have sufficient understanding to modify the previously described memory device embodiment to implement embodiments 20 of the mode entry circuit. For example, the mode entry circuit 414 is represented in Figure 4 as a separate circuit block. However, the mode entry circuit 414 may be incorporated into one of the other circuit blocks, or alternatively, may be split among several circuit blocks. The particular arrangement of the mode entry circuit 414 within a memory device will be a matter of design preference. Additionally, although initiation of a mode of operation has 25 been described herein as being triggered by a relatively high voltage address signal or signals, it will be appreciated that other types of signals could be used to invoke the mode of operation as well. For example, control signals could be provided to the mode entry circuit 414 in addition to or instead of the address signals, as previously discussed, and

used to trigger a mode of operation. Such types of modifications may be made without departing from the scope of the present invention.

Figure 5 is a block diagram of a computer system 500 including computing circuitry 502. The computing circuitry 502 contains a memory device 501 that includes a mode entry circuit according to an embodiment of the present invention. The computing circuitry 502 performs various computing functions, such as executing specific software to perform specific calculations or tasks. In addition, the computer system 500 includes one or more input devices 504, such as a keyboard or a mouse, coupled to the computer circuitry 502 to allow an operator to interface with the computer system. Typically, the computer system 500 also includes one or more output devices 506 coupled to the computer circuitry 502, such output devices typically being a printer or a video terminal. One or more data storage devices 508 are also typically coupled to the computer circuitry 502 to store data or retrieve data from external storage media (not shown). Examples of typical storage devices 508 include hard and floppy disks, tape cassettes, and compact disc read-only memories (CD-ROMs). The computer circuitry 502 is typically coupled to the memory device 501 through appropriate address, data, and control busses to provide for writing data to and reading data from the memory device 501.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.